PATENT ABSTRACTS OF JAPAN

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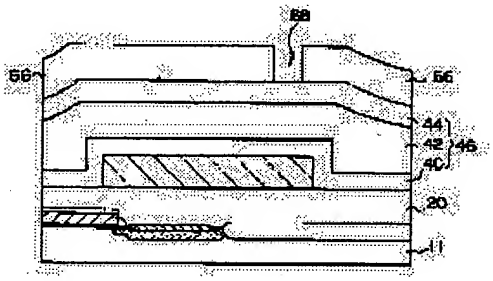
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To increase the degree of freedom of isotropic etching by constituting an interlayer insulating film by forming a first silicon oxide film by causing a silicon compound and hydrogen peroxide to react with each other by the CVD method and forming a second silicon oxide film which becomes a cap layer on the first silicon oxide film.
SOLUTION: A third silicon oxide film 40 is formed by causing tetraethoxysilane and oxygen to react with each other by the plasma CVD method. Then, under a reduced pressure, a first silicon oxide film 42 is formed by causing SiH4 and H2O2 to react with each other by the CVD method by using a nitrogen gas as a carrier. The silicon oxide film 42 has a film thickness larger than at least the step of the underlying third silicon oxide film 40. After the moisture in the first silicon oxide film 42 is removed more or less, a second silicon oxide film 44 is successively formed by causing gasses to react with each other under the presence of SiH4, PH3, and N2O by the plasma CVD method.



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CLAIMS

[Claim(s)]

[Claim 1] Having the semiconductor substrate which has the main front face, and the layer insulation film which is located on the aforementioned main front face and has a through hole, the aforementioned through hole is the manufacture method containing the wall inserted in the upper surface section, the inferior-surface-of-tongue section, and the aforementioned upper surface section and the aforementioned inferior-surface-of-tongue section of a semiconductor device, and includes the following processes.

The process which forms the aforementioned through hole characterized by providing the following. (a) The process, the (b) silicon compound which form the 1st silicon oxide which a silicon compound and a hydrogen peroxide are made to react by CVD, and constitutes the aforementioned layer insulation film. At least one sort of the compound containing oxygen and oxygen. The aforementioned wall which has the taper section to which the aforementioned through hole becomes small as isotropic etching of the process, the 1st silicon oxide of (c) above, and the 2nd silicon oxide of the above which form the 2nd porous silicon oxide which is made to react by ** CVD, and constitutes the aforementioned layer insulation film, and serves as a cap layer on the silicon oxide of the above 1st is carried out alternatively and it goes to the aforementioned inferior-surface-of-tongue section from the aforementioned upper surface section.

[Claim 2] The manufacture method of a semiconductor device which includes the process which anneals the aforementioned layer insulation film at 350-500 degrees C between the aforementioned process (b) and the aforementioned process (c) in a claim 1.

[Claim 3] It is the manufacture method of a semiconductor device which the aforementioned layer insulation film is located under the silicon oxide of the above 1st in a claim 1 or 2, and a kind is made to react by CVD at least, and includes the process of a silicon compound and the compound containing oxygen and oxygen which forms the 3rd silicon oxide of the above in front of the aforementioned process (a) including the 3rd silicon oxide used as a base layer.

[Claim 4] The claims 1 and 2 or 3 characterized by providing the following. The aforementioned through hole is the lower part. The upper part which is located on it and contains the aforementioned taper section. It is the process which shell composition is carried out, and the aforementioned process (c) carries out isotropic etching of the 1st silicon oxide of the above, and the 2nd silicon oxide of the above alternatively, and forms the aforementioned upper part. The process which carries out anisotropic etching of the aforementioned layer insulation film located under the aforementioned upper part alternatively, and forms the aforementioned lower part.

[Claim 5] The manufacture method of a semiconductor device which wiring is formed on the aforementioned layer-insulation film, and includes the process which forms the barrier layer which becomes a part [the aforementioned wiring] after the aforementioned process (c) on the front face of the aforementioned through hole, and the front face of the aforementioned layer-insulation film, and the process which forms in the front face of the aforementioned barrier layer the electric-conduction film which becomes a part [the aforementioned wiring] in claims 1, 2, and 3 or 4.

[Claim 6] It is the manufacture method of a semiconductor device which forms the 1st aluminum film which consists of an alloy which the aforementioned electric conduction film is 200 degrees C or less in temperature in a claim 5, and makes aluminum or aluminum a principal component, and forms after that the 2nd aluminum film which consists of an alloy which is 300 degrees C or more in temperature, and mak s aluminum or aluminum a principal component.
[Claim 7] the aforementioned silicon compound used at the aforementioned process (a) in claims 1, 2, 3, 4, and 5 or 6 — a mono silane, a disilane, and SiH2 — the manufacture method of a semiconductor device which is at least one sort chosen from organic silane compounds, such as inorganic silane compounds, such as Cl2 and SiF4, and CH3SiH3, dimethylsilane, a TORIPURO pill silane, and a tetrapod ethoxy silane
[Claim 8] The aforementioned process (a) is the manufacture method of a semiconductor device which the aforementioned silicon compound is an inorganic silane compound in a claim 7, and is performed by reduced pressure CVD under 0–20–degree C temperature conditions.
[Claim 9] The aforementioned process (a) is the manufacture method of a semiconductor device which the aforementioned silicon compound is an organic silane compound in a claim 7, and is performed by reduced pressure CVD under 0–150–degree C temperature conditions.
[Claim 10] It is the manufacture method of a semiconductor device that the aforementioned process (b) is performed by the plasma CVD method under 300–450–degree C temperature conditions in claims 1, 2, 3, 4, 5, 6, 7, and 8 or 9.
[Claim 11] The compound which contains the aforementioned oxygen used at the aforementioned process (b) in a claim 10 is the manufacture method of a semiconductor device which is a dinitrogen oxide.
[Claim 12] It is the manufacture method of a semiconductor device that the aforementioned process (b) is performed by ordinary–pressure CVD under 300–550–degree C temperature conditions in claims 1, 2, 3, 4, 5, 6, 7, and 8 or 9.
[Claim 13] The compound which contains the aforementioned oxygen used at the aforementioned process (b) in a claim 12 is the manufacture method of a semiconductor device which is ozone.
[Claim 14] The manufacture method of a semiconductor device of exposing the 1st silicon oxide of the above to ozone atmosphere in claims 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, and 12 or 13 before forming the 2nd silicon oxide of the above at the aforementioned process (b).
[Claim 15] The semiconductor device equipped with the semiconductor substrate which is characterized by providing the following and which has the main front face, and the layer insulation film located on the aforementioned main front face. The aforementioned layer insulation film is the 1st silicon oxide formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide. The 2nd silicon oxide which is located on the silicon oxide of the above 1st and constitutes a cap layer. It is formed in the 1st silicon oxide of the above, and the 2nd silicon oxide of the above, and ****** and the aforementioned layer insulation film are the upper surface section. The wall inserted in the inferior–surface–of–tongue section, and the aforementioned upper surface section and the aforementioned inferior–surface–of–tongue section.
[Claim 16] It is the semiconductor device which the aforementioned layer insulation film is located under the silicon oxide of the above 1st in a claim 15, and contains the 3rd silicon oxide which constitutes a base layer.
[Claim 17] It is the semiconductor device by which shell composition is carried out with the upper part which the aforementioned through hole is located on it with the lower part in a claim 15 or 16, and contains the aforementioned taper section.
[Claim 18] The aforementioned wiring is a semiconductor device containing the electric conduction film formed in the front face of the barrier lay r formed in the front face of the aforementioned through hole, and the front face of the aforementioned layer insulation film, and the aforementioned barrier layer including the wiring formed on the aforementioned layer insulation film in claims 15 and 16 or 17.
[Claim 19] It is the semiconductor device with which the aforementioned electric conduction film makes aluminum or aluminum a principal component in a claim 18.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to a semiconductor device and its manufacture method.
[0002]
Background Art and Problem(s) to be Solved by the Invention] The layer insulation film used for production of a semiconductor device may consist of two or more films. Such a layer insulation film is indicated by JP,4-218947,A etc. For example, there are a cap layer which consists of the base layer which consists of a silicon oxide, an SOG film located on a base layer, and a silicon oxide located on an SOG film, and a layer insulation film by which shell composition is carried out. It is made for the wall of the through hole formed in this layer insulation film to have the taper section. It is for making good coverage of the electric conduction film with which a through hole is filled up.
[0003] As the formation method of the through hole of such a configuration, first, isotropic etching of the layer insulation film is carried out alternatively, and this etching is stopped on the way. Since it is isotropic etching, as for a layer insulation film, a longitudinal direction besides lengthwise is also deleted. The amount deleted by the longitudinal direction increases, so that it goes to the upper surface section of a through hole. Therefore, it becomes the wall which has the taper section. Next, it changes to anisotropic etching and the remaining layer insulation films are **********ed alternatively. A through hole is completed according to the above process.
[0004] By the way, the etch rate of an SOG film is quite larger than that of a cap layer. For this reason, when even an SOG film carries out isotropic etching, the longitudinal direction of an SOG film **********s superfluously. Thereby, a crevice is made to the wall of a through hole.
[0005] For the above reason, isotropic etching was stopped in the cap layer. For this reason, the flexibility of isotropic etching was low. It occurred that follow, for example, an electric conduction film is not embedded at a through hole when an aspect ratio is a large through hole.
[0006] The purpose of this invention is offering the semiconductor device manufactured by the manufacture method of the semiconductor device which the flexibility of isotropic etching increases, and its method.
[0007]
[Means for Solving the Problem] this invention is located on the semiconductor substrate which has the main front face, and the main front face, and it has the layer insulation film which has a through hole, and a through hole is the manufacture method containing the wall inserted in the upper surface section, the undersurface section, and the upper surface section and the undersurface section of a semiconductor device, and includes the following processes.
[0008] (a) The process and th (b) silicon compound which form the 1st silicon oxide which a silicon compound and a hydrogen peroxide are made to r act by CVD, and constitutes a layer insulation film, At least one sort of the compound containing oxygen and oxygen is made to react by CVD. The 2nd porous silicon oxide which constitutes a layer insulation film and serves as a cap layer The process which forms the through hole containing the wall which has the taper section to which a through hole becomes small as isotropic etching of the process formed on the

1st silicon oxide, the (c) 1st silicon oxide and, and the 2nd silicon oxide is carried out alternatively and it goes to the undersurface section from the upper surface section.
[0009] The semiconductor device produced by the manufacture method of this invention is equipped with the semiconductor substrate which has the main front face, and the layer insulation film located on the main front face. A layer insulation film contains the 1st silicon oxide formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide, and the 2nd silicon oxide which is located on the 1st silicon oxide and constitutes a cap layer. A layer insulation film is formed in the 1st silicon oxide and the 2nd silicon oxide, and contains the through hole which has the wall inserted in the upper surface section, the undersurface section, and the upper surface section and the undersurface section. A wall has the taper section to which a through hole becomes small as it goes to the undersurface section from the upper surface section.
[0010] The manufacture method of this invention forms the 1st silicon oxide according to the process (a) instead of an SOG film. It turns out that the speed of the isotropic etching of the 1st silicon oxide is almost the same similarly [to the speed of the isotropic etching of the 2nd silicon oxide]. For this reason, the 1st silicon oxide can also carry out isotropic etching. Therefore, according to the manufacture method of this invention, the flexibility of isotropic etching can be made to increase.
[0011] The speed of the isotropic etching of the 2nd silicon oxide needs to be the same as the speed of the isotropic etching of the 1st silicon oxide, and almost the same. Such 2nd silicon oxide can be formed with the usual CVD, for example, the thermal decomposition method of a silane compound, and a adding-water part solution method. The 2nd silicon oxide can be formed by ordinary-pressure CVD, the plasma CVD method, or reduced pressure CVD.
[0012] To the 2nd silicon oxide which is porosity, it is more desirable impurities, such as Lynn and boron, and that Lynn is added preferably. It is because the layer which can ease the stress of this film and cannot break soft further easily moderately so to speak can be constituted from weakening the bonding strength between Si-O molecules of the silicon oxide which constitutes this film. Moreover, there is a function as a getter of a movable ion in which impurities, such as Lynn included in this silicon oxide, have a bad influence on the reliance property of elements, such as alkali ion, as an important role of the 2nd silicon oxide. The concentration of the impurity contained in the 2nd silicon oxide is 1 - 6 % of the weight preferably, when the point of the stress relaxation of the gettering function mentioned above or a film is taken into consideration.
[0013] Moreover, the 2nd silicon oxide also has the function to prevent moisture absorption of the 1st silicon oxide. Furthermore, the 2nd silicon oxide has compressive internal stress. Therefore, when other films which constitute a layer insulation film have the internal stress of hauling, it can be eased and it can prevent a crack occurring on a layer insulation film.
[0014] Moreover, as for the plasma CVD method when forming this 2nd silicon oxide, it is desirable under 300-450-degree C temperature conditions to be carried out by the RF. It is because there is the desorption effect of the moisture in the 1st silicon oxide.
[0015] Although O2 is sufficient as the compound containing the oxygen used when forming the 2nd silicon oxide, it is desirable that it is a dinitrogen oxide (N2O). Since the dinitrogen oxide of the plasma state tends to react by using a dinitrogen oxide as reactant gas with the hydrogen bond (-H) of the silicon compound which constitutes the 1st silicon oxide, while forming the 2nd silicon oxide, desorption of the gasification component (hydrogen, water) of the 1st silicon oxide can be promoted.
[0016] Formation of the 2nd silicon oxide may be performed by ordinary-pressure CVD under 300-550-degree C temperature conditions instead of a plasma CVD method. In this case, as for the compound containing the oxygen used when forming the 2nd silicon oxide, it is desirable that it is ozone.
[0017] Furthermore, before forming the 2nd silicon oxide, it is desirable to expose the 1st silicon oxide to ozone atmosphere. Since ozone tends to react by passing through this process with the hydrogen bond (-H) of a silicon compound and the hydroxyl group (-OH) which constitute the 1st silicon oxide, the hydrogen in the 1st silicon oxide and desorption of water can be promoted.
[0018] Moreover, the thickness of the 2nd silicon oxide is 100nm or more preferably, when the

point of prevention of flat nature and a crack and the thickness of a layer insulation film is taken into consideration.

[0019] Moreover, in the manufacture method of this invention, a silicon compound and a hydrogen peroxide are made to react by CVD, and the 1st silicon oxide is formed. Thereby, the layer insulation film which was excellent in flat nature can be formed. That is, the 1st silicon oxide formed by the manufacture method of this invention has the self-flattening property of having a high fluidity and having excelled in itself. If the mechanism makes a silicon compound and a hydrogen peroxide react by CVD, it will be considered to be because for a silanol to be formed into a gaseous phase, and for a fluid good film to be formed when this silanol deposits on a wafer front face.

[0020] For example, when a mono silane is used as a silicon compound, a silanol is formed at the reaction shown by the following formula (1), (1)', etc.

[0021] Formula (1)

SiH4+2H2O2 -> Si(OH)4+2H2 formula (1) The silanol formed by 'SiH4+3H2O2 -> Si(OH)4+2H2 O+H2 and the formula (1), and (1)' serves as a silicon oxide, when water ****s at the polycondensation reaction shown by the following formula (2).

[0022] Formula (2)

Si(OH)4 -> as the SiO2+2H2O above-mentioned silicon compound — a mono silane, a disilane, and SiH2 — organic silane compounds, such as inorganic silane compounds, such as Cl2 and SiF4, and CH3SiH3, dimethylsilane, a TORIPURO pill silane, and a tetrapod ethoxy silane, etc. can be illustrated

[0023] Moreover, under 0-20-degree C temperature conditions, when the above-mentioned silicon compound is an inorganic silicon compound, when the above-mentioned silicon compound is an organic silicon compound, it is desirable [a process (a)] to be carried out by reduced pressure CVD under 0-150-degree C temperature conditions. If temperature is higher than the above-mentioned upper limit, when the polycondensation reaction of the above-mentioned formula (2) progresses too much, the 1st silicon oxidization membrane fluidity will become low, and good flat nature will be hard to be obtained at this membrane formation process. Moreover, there is un-arranging [to which adsorption of a low and the decomposition moisture within a chamber and dew condensation out of a chamber occur, and it becomes difficult from the above-mentioned lower limit for membrane formation equipment to control temperature].

[0024] As for the 1st silicon oxide formed of this invention, it is desirable to be formed by the thickness of the grade which can fully cover the level difference of a ground. The thickness of the 1st silicon oxide is 300-1500nm preferably, although the lower limit is dependent on the height of the irregularity of a ground. When the thickness of the 1st silicon oxide exceeds the above-mentioned upper limit, a crack may be produced for the stress of the film itself.

[0025] In the manufacture method of this invention, it is desirable to include the process which anneals a layer insulation film at 350-500 degrees C between processes (b) (c).

[0026] In the case of the structure where a layer insulation film contains the 3rd silicon oxide (base layer) located under the 1st silicon oxide, the manufacture method of this invention has the following desirable modes. That is, it is desirable to include the process of a silicon compound and the compound containing oxygen and oxygen which a kind is made to react by CVD at least, and forms the 3rd silicon oxide in front of a process (a).

[0027] This base layer has the passivation function which neither moisture nor an excessive impurity moves, and the function which raises the adhesion of the layer under a base layer (it is the main front face of a semiconductor substrate when there is no layer in the bottom of a base layer), and the 1st silicon oxide from the 1st silicon oxide in the layer under a base layer (when there is no layer in the bottom of a base layer, it is the main front face of a semiconductor substrate).

[0028] Moreover, when the gettering effect over alkali ion is required, a means to form the PSG film which includes Lynn one to 6% of the weight between a means to add impurities, such as Lynn, one to 6% of the weight or the 3rd silicon oxide, and the 1st silicon oxide into the 3rd silicon oxide which constitutes a base layer can be adopted.

[0029] As for a process (c), in the manufacture method of this invention, it is desirable to include

the process which forms the upper part of the through hole which carries out isotropic etching of the 1st silicon oxide and the 2nd silicon oxide alternatively, and contains the taper section, and the process which carries out anisotropic etching of the layer insulation film located under the upper part alternatively, and forms the lower part of a through hole. in addition, the upper part of a through hole does not need to reach the 3rd silicon oxide That is, the boundary of the upper part of a through hole and the lower part means that you may be in the formation position of the 3rd silicon oxide, and may be in the formation position of the 1st silicon oxide.
[0030] Shell composition of the through hole of the layer insulation film of the semiconductor device manufactured by the manufacture method of this invention is carried out with the lower part and the upper part which is located on it and contains the taper section.
[0031] In the manufacture method of this invention, it is desirable to include the process which forms the barrier layer which becomes a part [wiring] after a process (c) on the front face of a through hole and the front face of a layer insulation film, and the process which forms in the front face of a barrier layer the electric conduction film which becomes a part [wiring].
[0032] In the semiconductor device manufactured by the manufacture method of this invention, a layer insulation film has a through hole. Further, this semiconductor device is formed in the front face of a through hole, and the front face of a layer insulation film, is formed in the front face of the barrier layer which becomes the part and barrier layer of wiring, and contains the electric conduction film which becomes a part [wiring].
[0033] In the manufacture method of this invention, the formation process of an electric conduction film has the following desirable processes. In the above-mentioned through hole, the 1st aluminum film which consists of an alloy which makes aluminum or aluminum a principal component at the temperature of 200 degrees C or less first is formed, and the 2nd aluminum film which consists of an alloy which makes aluminum or aluminum a principal component at the temperature of 300 degrees C or more is formed after that.
[0034] As an alloy which makes the above-mentioned aluminum a principal component, at least one sort chosen from copper, silicon, germanium, magnesium, cobalt, beryllium, etc. of 2 yuan or 3 yuan or more alloys can be illustrated.
[0035]
[Embodiments of the Invention] [The gestalt of the 1st operation]
{Explanation of structure} drawing 1 is cross-section structural drawing of the semiconductor device concerning the gestalt of operation of the 1st of this invention. The structure of the semiconductor device concerning the gestalt of the 1st operation is explained briefly. The MOS field effect transistor which has the gate electrode 14 is formed in the main front face of a silicon substrate 11. The layer insulation film 20 is formed on the main front face of a silicon substrate 11 so that a MOS field effect transistor may be covered.
[0036] The 1st metal wiring layer 38 is formed on the layer insulation film 20. The layer insulation film 46 is formed on the layer insulation film 20 so that the 1st metal wiring layer 38 may be covered. The layer insulation films 46 are three layer structures.
[0037] That is, the 3rd silicon oxide 40 which is a base layer is in the lowest layer. The 1st silicon oxide 42 is located on the 3rd silicon oxide 40. The 1st silicon oxide 42 is formed of the polycondensation reaction of a silicon compound and a hydrogen peroxide. The 2nd silicon oxide 44 which is a cap layer is located on the 1st silicon oxide 42.
[0038] The through hole 48 which reaches the 1st metal wiring layer 38 is formed in the layer insulation film 46. Shell composition of the through hole 48 is carried out with the lower part 51 and the upper part 49 whose wall is the taper section. The taper section said here is a portion to which a through hole 48 becomes small as it goes to the inferior-surface-of-tongue section from the upper surface section of a through hole 48 among the walls of a through hole 48. In addition, in the lower part 51, it is changeless in the size of a through hole 48.
[0039] The 2nd metal wiring layer 64 is formed on the layer insulation film 46. The 1st metal wiring layer 38 and the 2nd metal wiring layer 64 are electrically connected by the electric conduction film containing the aluminum film with which the through hole 48 was filled up.
[0040] {Explanation of the manufacture method}, next the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention are

explained. Drawing 2 - drawing 8 are cross-section structural drawings for explaining this in order of a process.
[0041] (Formation of an element) As shown in drawing 2 , a MOS field effect transistor is formed in a silicon substrate 11 by the method generally used first. Specifically, the field insulator layer 12 is formed of selective oxidation on a silicon substrate 11, and the gate oxide film 13 is formed in an active field. The gate electrode 14 is formed by carrying out the spatter of the tungsten silicide on the polysilicon contest film into which SiH4 was pyrolyzed and was grown up, carrying out the laminating of the silicon oxide 18 further, and **********ing to a predetermined pattern further by channel pouring, after adjusting threshold voltage.
[0042] Subsequently, the low concentration impurity layer 15 of a source field or a drain field is formed by carrying out the ion implantation of Lynn. Subsequently, after the side-attachment-wall spacer 17 which becomes the side of the gate electrode 14 from a silicon oxide is formed, the high concentration impurity layer 16 of a source field or a drain field is formed by carrying out the ion implantation of the arsenic and activating an impurity by annealing processing using the halogen lamp.
[0043] Next, a predetermined silicon-substrate field is exposed by forming a CVD silicon oxide 100nm or less, and **********ing this film alternatively with the mixed-water solution of HF and NH4F. then — for example, the main front face of the silicon substrate which carried out by carrying out the spatter of the titanium by about 30-100nm thickness, and performing moment annealing for several seconds - about 60 seconds at the temperature of 650-750 degrees C into the nitrogen-gas-atmosphere mind which controlled oxygen to 50 ppm or less — the monochrome silicide layer of titanium — a silicon-oxide 18 top — titanium — a rich titanium night RAIDO (TiN) layer is formed Subsequently, if immersed into NH4OH and the mixed-water solution of H2O2, etching removal of the aforementioned titanium night RAIDO layer will be carried out, and the monochrome silicide layer of titanium will remain only in the main front face of a silicon substrate. Furthermore, perform 750-850-degree C lamp annealing, the aforementioned monochrome silicide layer is made to form into die silicide, and the titanium silicide layer 19 is formed in the front face of the high concentration impurity layer 16 at a self-adjustment target.
[0044] In addition, when the gate electrode 14 is formed only with contest polysilicon and it is made to expose by selective etching, both a gate electrode, source, and drain field become the CHITANSA LISA id structure separated with the side-attachment-wall spacer.
[0045] In addition, the Salicide structure may consist of tungsten silicide and molybdenum silicide instead of titanium silicide.
[0046] Next, as shown in drawing 3 , the layer insulation film 20 containing a silicon oxide is formed by CVD. Well-known conditions can be used for formation conditions. Structure is much more sufficient as the layer insulation film 20, and multilayer structure is sufficient as it.
[0047] And the 1st metal wiring layer 38 containing an aluminum film is formed by the sputtering method on the layer insulation film 20. Structure is much more sufficient as the 1st metal wiring layer 38, and multilayer structure is sufficient as it.
[0048] (Formation of the layer insulation film 46)
a. **** of the 3rd silicon oxide 40 — the 3rd silicon oxide 40 of 50-200nm of thickness is first formed by making a tetrapod ethoxy run (TEOS) and oxygen react by the plasma CVD method at 300-500 degrees C This silicon oxide 40 does not have oxidization or the dregs ping of the 1st metal wiring layer 38, either, and its insulation is also high, and its etch rate to the solution of hydrogen fluoride is also slow, and it turns into a precise film from the film grown up from SiH4.
[0049] b. Form the 2.5x102Pa or less of the 1st silicon oxide 42 preferably formation of the 1st silicon oxide 42, next by making SiH4 and H2O2 react by CVD by using nitrogen gas as a carrier more preferably under reduced pressure of 0.3x102 to 2.0x102Pa. The 1st silicon oxide 42 is formed by the thickness which has larger thickness than the level difference of the 3rd lower layer silicon oxide 40 at least, that is, fully covers this level difference. Moreover, the upper limit of the thickness of the 1st silicon oxide 42 is set as the grade which a crack does not produce in this film. Specifically, in order to obtain better flat nature, as for the thickness of the 1st silicon oxide 42, it is desirable that it is thicker than a lower layer level difference, and it is preferably

set as 300–1500nm.
[0050] Since it participates in the fluidity at the time of membrane formation of this film, membrane fluidity will fall if membrane formation temperature is high, and the membrane formation temperature of the 1st silicon oxide 42 spoils flat nature, 0–20 degrees C of temperature at the time of membrane formation are more preferably set as 0–10 degrees C.
[0051] Moreover, although especially the flow rate of H2O2 is not restricted, it is desirable that concentration is 55 to 65 volume %, for example, and it is a flow rate more than the double precision of SiH4, and it is desirable to be set, for example as the flow rate range of 100 – 1000SCCM by gas conversion from membranous homogeneity and the point of a throughput.
[0052] The 1st silicon oxide 42 formed at this process is in the state of silanol polymer, and a fluidity is good and has a high self–flattening property. Moreover, since many hydroxyl groups (–OH) are included, the 1st silicon oxide 42 has hygroscopicity in a high state.
[0053] c. Put under existence of SiH4, PH3, and N2O continuously after leaving it for 30 – 120 seconds under reduced pressure within formation, next the chamber of the 2nd silicon oxide 44 and removing some moisture in the 1st silicon oxide 42. By making gas react by the plasma CVD method at the temperature of 300–450 degrees C at 200–600kHz high frequency, the PSG film (the 2nd silicon oxide) 44 of 100–600nm of thickness is formed. As for this 2nd silicon oxide 44, it is desirable to be formed after being saved in the atmosphere in which the hygroscopicity of the 1st silicon oxide 42 of the above is continuously formed in in consideration of a high thing following formation of the 1st silicon oxide 42 of the above, or the 1st silicon oxide 42 does not contain moisture.
[0054] Moreover, the 2nd silicon oxide 44 needs that desorption of gasification components, such as water contained in the 1st silicon oxide 42 of the above by the annealing processing performed behind and hydrogen, is easy, and to be porous (porosity) in consideration of fully being carried out. For that purpose, temperature is desirable and it is preferably [more] desirable [the 2nd silicon oxide 44] 1MHz or less preferably to form membranes by the 200–600kHz plasma CVD method more preferably, and to include impurities, such as Lynn, 300–400 degrees C 450 degrees C or less. By containing such an impurity in the 2nd silicon oxide 44, it will be in a more nearly porous state and the 2nd silicon oxide 44 not only can ease the stress to a film, but can have the gettering effect over alkali ion etc. with it. The concentration of such an impurity is set up in consideration of points, such as the gettering effect and stress–proof nature. For example, when an impurity is Lynn, it is desirable to be contained at 2 – 6% of the weight of a rate.
[0055] Moreover, in plasma CVD, desorption of the hydrogen bond in the 1st silicon oxide 42 is promoted by using N2O as a compound containing oxygen. Consequently, gasification components, such as moisture contained in the 1st silicon oxide 42 and hydrogen, can be removed more certainly.
[0056] In consideration of the role which adjusts the thickness of the layer insulation film needed, and the function by which N2O plasma is desorbed from hydrogen bond, 100nm or more of thickness of this 2nd silicon oxide 44 is more preferably set as 200–600nm.
[0057] d. Perform annealing processing at the temperature of 350–500 degrees C in annealing processing, next nitrogen–gas–atmosphere mind. By this annealing processing, the 1st silicon oxide 42 of the above and the 2nd silicon oxide 44 turn precisely more, and have good insulation and good water resistance. That is, by setting an annealing temperature as 350 degrees C or more, the condensation polymerization reaction of the silanol in the 1st silicon oxide 42 is performed nearly completely, and the water and hydrogen which are contained in this film are fully emitted, and can form a precise film. Moreover, it does not have a bad influence on the aluminum film which constitutes the 1st metal wiring layer 38 by setting an annealing temperature as 500 degrees C or less. As long as it is allowed, the higher one of an annealing temperature is desirable. Because, it is the shell in which a layer insulation film cannot receive a bad influence easily due to the insulating improvement in (1) layer insulation film, and heat treatment in (2) back processes.
[0058] In annealing processing, in order to make small influence of a heat strain to the 1st silicon oxide 42, it is more desirable to perform run ping annealing which raises the temperature of a

wafer gradually or continuously.
[0059] In addition, when the layer insulation film 46 is between the main front face of a silicon substrate 11, and the 1st metal wiring layer 38 (formation position of the layer insulation film 20), annealing processing can be performed above 500 degrees C. It is because aluminum wiring is not formed.
[0060] (Formation of a through hole) As shown in drawing 5 , a resist 66 is formed on the layer insulation film 46. And selection exposure is carried out, a resist 66 is developed, and opening 68 is formed.
[0061] As shown in drawing 6 , isotropic etching of the layer insulation film 46 is alternatively carried out using the solution containing HF. This etching is stopped in the middle of etching of the 1st silicon oxide 42. Thereby, the upper part 49 of a through hole is formed. The wall of the upper part 49 serves as the taper section. Following (1) and (2) can be illustrated as conditions.
[0062] Conditions (1)
Etching reagent Temperature of HF:NH4 F-1:6 etching reagent Annealing temperature of the room temperature layer insulation film 46 450 degrees C of etch rates of the 1st silicon oxide 42 and the 2nd silicon oxide 44 were about 4.3nm/second under these conditions.
[0063] Conditions (2)
Etching reagent Temperature of HF:NH4 F-1:20 etching reagent Annealing temperature of the room temperature layer insulation film 46 450 degrees C of etch rates of the 1st silicon oxide 42 and the 2nd silicon oxide 44 were about 1.1nm/second under these conditions.
[0064] As shown in drawing 7 , anisotropic etching of the layer insulation film 46 under the upper part 49 is carried out alternatively. By this etching, a part of 1st metal wiring layer 38 is exposed. Thereby, the lower part 51 of a through hole is formed. The following can be illustrated as conditions.
[0065]
Etching system Reactive ion etching system Etching gas CF4 and CHF3 (Ar, helium, or Ne as inert gas)
temperature in a chamber Room temperature -100 degree C Chamber internal pressure 0.02 - 0.5torr RF power 300-1000w — the etch rate of the 1st silicon oxide 42 and the 3rd silicon oxide 40 was 8-11nm/second under these conditions
[0066] And the resist 66 was removed.
[0067] By the above isotropic etching and anisotropic etching, the through hole 48 which has the taper section is completed. In the through hole 48 which carried out such a configuration, good deposition of an aluminum film is possible so that it may mention later.
[0068] (Degasifying processing) ****** which includes a degasifying process first — it ****** just a lamp chamber — the base pressure of 1.5x10 - 4 or less Pa — 150-350 degrees C (heat treatment A) of lamp heating for 30 - 60 seconds are preferably given at the temperature of 150-250 degrees C Subsequently, degasifying processing is performed by introducing argon gas by another chamber by the pressure of 1x10-1 to 15x10 to 1 Pa, and performing heat treatment for 30 - 300 seconds (degasifying process; heat treatment B) at the temperature of 300-500 degrees C.
[0069] In this process, the moisture adhering to the wafer etc. is removable by mainly heat-treating the whole wafer including the rear face and the side of a wafer in heat treatment A first.

[0070] Furthermore, in heat treatment B, the gasification component in the 1st silicon oxide 42 which constitutes the layer insulation film 46 (H, H2O) is mainly removable. Consequently, generating of the gasification component from the layer insulation film 46 can be prevented at the time of formation of the barrier layer of the following process, and an aluminum film.
[0071] In the form of this operation, since it dissolves the gasification component (O, H, H2 O, N) of dozens atom %, before a WETTENGU layer, for example, Ti film, forms this film, it is very effective [film] to remove the gasification component in the layer insulation film 46, when forming the aluminum film within a through hole 48 good. If the gasification component in the layer insulation film 46 of the low rank of a WETTENGU layer is not fully removed, at the temperature at the time of formation of a WETTENGU layer (usually 300 degrees C or more), the

gasification component in the layer insulation film 46 will be emitted, and this gas will be incorporated in a WETTENGU layer. Furthermore, in order that this gas may secede from a WETTENGU layer at the time of membrane formation of an aluminum film and may come out to the interface of a WETTENGU layer and an aluminum film, it has a bad influence on the adhesion of an aluminum film, or a fluidity.

[0072] (Membrane formation of a WETTENGU layer) As shown in drawing 8 , a titanium film is formed by 20–70nm thickness by the spatter as a film which constitutes the WETTENGU layer 50. The temperature of a spatter is chosen in 200–450 degrees C according to thickness.

[0073] (Degasifying processing before membrane formation of an aluminum film, and cooling of a wafer) First, as shown in drawing 8 , before cooling a wafer, heat treatment for 30 – 60 seconds (heat treatment C) is performed in a lamp chamber at the base pressure of 1.5x10 – 4 or less and the temperature of 150–250 degrees C, and matter, such as water adhering to the substrate, is removed. Then, before forming an aluminum film, 100 degrees C or less of substrate temperature are preferably lowered to ordinary temperature –50 degree C temperature. This cooling process is important in order to lower the substrate temperature which rose with the above–mentioned heat treatment C, for example, on the stage which has a water–cooled function, lays a wafer and lowers this wafer temperature to predetermined temperature.

[0074] Thus, in case the 1st aluminum film 52 is formed by cooling a wafer, the layer insulation film 46 and the WETTENGU layer 50, and capacity further emitted from the whole wafer surface can be lessened as much as possible. Consequently, the influence of gas detrimental to the coverage nature and adhesion which stick to the interface of the WETTENGU layer 50 and the 1st aluminum film 52 can be prevented.

[0075] (Membrane formation of an aluminum film) As shown in drawing 8 , first, it is 30–100 degrees C in temperature more preferably, and the aluminum containing 0.2 – 1.0% of the weight of copper is formed at high speed by the spatter by 150–300nm of thickness, and 200 degrees C or less of 1st aluminum film 52 are formed. Then, it heats in substrate temperature of 420–460 degrees C within the same chamber, the aluminum which contains copper similarly is formed by the low speed by the spatter, and the 2nd aluminum film 54 of 300–600nm of thickness is formed. Here, in membrane formation of an aluminum film, although neither membrane formation conditions nor the design matter of a device manufactured can prescribe "high speed" generally, a sputtering rate 10nm [/second] or more is meant about, and a "low speed" means a sputtering rate 3nm [/second] or less about.

[0076] An example of the sputtering system for forming the 1st and 2nd aluminum films 52 and 54 to drawing 9 is shown. This sputtering system has the electrode 57 which serves both as the target 56 which serves as an electrode in a chamber 55, and a stage. The substrate (wafer) W processed is installed on an electrode 57. The 1st gas supply way 58 is connected to a chamber 55, and the 2nd gas supply way 59 is connected to the electrode 57. Argon gas is supplied from [each] the gas supply ways 58 and 59. And the temperature of Wafer W is controlled by the gas supplied from the 2nd gas supply way 59. In addition, the means for discharging the gas in a chamber 55 is not illustrated.

[0077] An example which controlled substrate temperature using such a sputtering system is shown in drawing 10 . In drawing 10 , a horizontal axis shows elapsed time and a vertical axis shows substrate (wafer) temperature. Moreover, in drawing 10 , the line which the line shown with Sign a shows the substrate temperature change when setting the temperature of the stage 57 of a sputtering system as 350 degrees C, and is shown with Sign b shows change of the substrate temperature when raising the temperature of a stage 57 by supplying hot argon gas in a chamber through the 2nd gas supply way 59.

[0078] For example, the temperature control of a substrate is performed as follows. First, the temperature of a stage 57 is beforehand set as the temperature (350–500 degrees C) for forming the 2nd aluminum film. In case the 1st aluminum film is formed, there is no supply of the gas from the 2nd gas supply way 59, and substrate temperature rises gradually by heating by the stage 57, as the sign a of drawing 10 shows. By supplying the gas heated through the 2nd gas supply way 59, in case the 2nd aluminum film is formed, substrate temperature rises rapidly and is controlled to become fixed at predetermined temperature so that the sign b of drawing 10

shows.
[0079] In the example shown in drawing 10 , stage temperature is set as 350 degrees C, while substrate temperature is set as 125–150 degrees C, the 1st aluminum film 52 is formed, and membrane formation of the 2nd aluminum film 54 is performed immediately after that.
[0080] In membrane formation of an aluminum film, control of the power impressed to a sputtering system with membrane formation speed and a substrate temperature control is also important. That is, although membrane formation speed is related, in case membrane formation of the 1st aluminum film 52 is performed by high power, the 2nd aluminum film 54 is performed by low power and it switches to low power from still higher power, it is important not to make power into zero. If power is made into zero, an oxide film will be formed in the bottom of reduced pressure on the front face of the 1st aluminum film, the wettability of the 2nd [to the 1st aluminum film] aluminum film will fall, and both adhesion will become bad. In other words, by always impressing power, supplying activity aluminum to the front face of the aluminum film under membrane formation can be continued, and formation of an oxide film can be suppressed. In addition, although the size of power cannot generally be specified depending on a sputtering system, membrane formation conditions, etc., in the case of the temperature conditions shown, for example in drawing 10 , it is desirable [a size] to set 5–10kW and low power as 300W–1kW for high power.
[0081] Thus, by forming continuously the 1st aluminum film 52 and the 2nd aluminum film 54 within the same chamber, control of temperature and power can be performed strictly and it becomes possible to form efficiently the aluminum film which is low temperature and was stabilized rather than before.
[0082] The thickness of the aluminum film 52 of the above 1st has desirable 100–300nm, for example, although the proper range is chosen from that a continuation layer can be formed and this aluminum film 52 by good step coverage in consideration of the ability to suppress discharge of the gasification component from lower layer WETTENGU layer 50 and layer insulation film 46. Moreover, although the 2nd aluminum film 54 is determined by the size of a through hole 48, its aspect ratio, etc., in order for an aspect ratio to fill a hole 0.5 micrometers or less about by three, for example, 300–800nm thickness is required for it.
[0083] (Membrane formation of an antireflection film) The antireflection film 62 of 30–80nm of thickness is formed by depositing TiN by the spatter by still more nearly another spatter chamber.
[0084] As shown in drawing 1 , after that, the deposit which consists of the aforementioned WETTENGU layer 50, the 1st aluminum film 52, the 2nd aluminum film 54, and an antireflection film 62 by the anisotropy dry etching system which makes the gas of Cl2 and BCl3 a subject is **********ed alternatively, and patterning of the 2nd metal wiring layer 64 is performed.
[0085] Thus, in the 2nd formed metal wiring layer 64, it was checked that aluminum is embedded by good step coverage, without generating a void in a through hole 48.
[0086] {Explanation of the main effects}
(1) According to the gestalt of the 1st operation, form the 1st silicon oxide 42 by making SiH4 and H2O2 react by CVD. The speed of the isotropic etching of the 1st silicon oxide 42 is the same as the 2nd silicon oxide 44 (cap layer) and it, and almost the same. For this reason, the 1st silicon oxide can also carry out isotropic etching. Therefore, according to the manufacture method of this invention, the flexibility of isotropic etching can be made to increase. If the flexibility of isotropic etching increases, the upper part 49 (a wall is the taper section) of a through hole 48 can be made deep. Therefore, aluminum can be embedded by good step coverage at a through hole 48, without generating a void. Moreover, thereby, the flat nature of the layer formed on this can be raised.
[0087] (2) According to the gestalt of the 1st operation, the layer insulation film 46 which has very good flat nature can be formed by forming the 1st silicon oxide 42 containing a silanol obtained by SiH4 and the reaction according H2O2 to CVD. Therefore, a process margin including processing of a wiring layer etc. can be made to be able to increase, and quality and the yield can be raised.
[0088] The following thing can be said when the layer insulation film 46 is especially formed

between the main front face of a silicon substrate 11, and the 1st metal wiring layer 38 (formation position of the layer insulation film 20). Since the layer insulation film 46 turns into a film by which flattening was considerably carried out at low temperature compared with the reflow temperature of the conventional BPSG film, it can improve a property in respect of a punch through, junction leak, etc., therefore can attain detailed-izing of an element, and reliable contact structure, and its manufacture process top is also advantageous.

[0089] (3) According to the gestalt of the 1st operation, by forming an aluminum film continuously [it is still more desirable and] within the same chamber including a degasifying process and a cooling process at least before the spatter of an aluminum film, it became possible to embed the through hole 48 to about 0.2 micrometers only by aluminum or the aluminium alloy, and improvement was able to be aimed at in respect of reliability and the yield. Moreover, there are also no copper segregation and unusual growth of crystal grain in the aluminum film which constitutes the contact section, and the good thing was checked also in respect of reliability including migration etc.

[0090] In the gestalt of the 1st operation, the following things besides the above-mentioned configuration of a through hole 48 can be considered as a reason the 1st and 2nd aluminum films 52 and 54 were embedded good at the through hole 48.

[0091] (a) By gasifying water and nitrogen which are contained in the layer insulation film 46 by performing a degasifying process, and fully emitting, in membrane formation of the 1st subsequent aluminum film 52 and 54, raised the adhesion of the WETTENGU layer 50 and the 1st aluminum film 52 by preventing generating of the gas from the layer insulation film 46 or the WETTENGU layer 50, and membrane formation of good step coverage was possible for.

[0092] (b) what the adhesion of the 1st aluminum film 52 was raised for in addition to the effect of the aforementioned degasifying process as the moisture or nitrogen which are contained in the layer insulation film 46 and the WETTENGU layer 50 in substrate temperature 200 degrees C or less by setting it as low temperature comparatively were not made to emit in membrane formation of the 1st aluminum film 52

[0093] (c) Since the 1st aluminum film 52 the very thing plays further the role which suppresses generating of the gas from a lower layer when substrate temperature goes up, the 2nd following aluminum film 54 can be formed at comparatively high temperature, and flow diffusion of the 2nd aluminum film can be performed good.

[0094] The gestalt] this invention of operation of others [ ] is not limited to the gestalt of implementation of the above 1st, but can replace the part with the following meanses.

[0095] {1} In the gestalt of the 1st operation, although the dinitrogen oxide was used as a compound containing oxygen at the time of membrane formation by the plasma CVD of the 2nd silicon oxide 44 instead, ozone can also be used. And before forming the 2nd silicon oxide 44, it is desirable to expose a wafer to ozone atmosphere.

[0096] For example, Wafer W is laid and it is made to move at the rate of predetermined using the belt furnace shown in drawing 11 onto the conveyance belt 80 heated by 400-500 degrees C at the heater 82. At this time, ozone is supplied from 1st gas head 86a, and the aforementioned wafer W is passed for the inside of 2 - 8% of the weight of ozone atmosphere over the time for 5 minutes or more. Subsequently, ozone, TEOS, and TMP (P(OCH3) 3) are mostly supplied by the ordinary pressure from the 2nd and 3rd gas heads 86b and 86c, and the PSG film (the 4th silicon oxide) 44 whose concentration of Lynn is 3 - 6 % of the weight is formed by 100-600nm of thickness. In addition, in drawing 11 , a sign 84 shows covering.

[0097] Thus, by using ozone instead of a dinitrogen oxide, the silicon oxide by TEOS can be formed by the ordinary pressure CVD. Moreover, membranes can be continuously formed efficiently by using a belt furnace.

[0098] Moreover, it was checked by the thermal-desorption spectrum (TDS) and the infrared spectroscopy (FTIR) by exposing Wafer W into ozone atmosphere that the flat nature of the layer insulation film 46 is good like the case where a dinitrogen oxide is used as that the 1st silicon oxide 42 has enough little hygroscopicity and moisture and reactant gas, and that a crack does not occur in the 1st silicon oxide 42.

[0099] {2} With the gestalt of the 1st operation, although the silicon oxide using TEOS by plasma

CVD was used as the 3rd silicon oxide 40, you may use a silicon oxide besides instead of for this (when it is in the formation position of the layer insulation film 20 especially). For example, the film formed by the elevated-temperature reduced pressure heat CVD using the mono silane and the dinitrogen oxide as such 3rd silicon oxide is sufficient. Membranes are faithfully formed to the shape of surface type of a ground, and not only coverage nature is good, but since this silicon oxide is precise, even if a passivation function is high and carries out the temperature up of it rapidly in annealing processing further, a crack cannot generate it easily in the 1st silicon oxide 42. Moreover, in order to use heat CVD, there is an advantage without a plasma damage. An elevated temperature here is a 700-850-degree C thing.

[0100] {3} With the gestalt of the 1st operation, although the layer insulation film 46 consists of silicon oxides of three layers, it may add not only this but other silicon oxides. For example, you may form the PSG film (concentration [of Lynn]; 1 - 6 % of the weight) of 100-300nm of thickness formed by the plasma CVD method between the 3rd silicon oxide 40 and the 1st silicon oxide 42. By putting in this PSG film, it was checked that the gettering function of a movable ion improves further. Moreover, the internal stress of the 1st silicon oxide 42 which acts on reduction and the 3rd silicon oxide 40 the internal stress of the 3rd silicon oxide 40 which acts on the 1st silicon oxide 42 can be decreased by putting in this PSG film.

[0101] Moreover, for example, when the flat nature of the 2nd silicon oxide 44 is inadequate, it can be performed as follows. A thick silicon oxide is formed on the 2nd silicon oxide 44, and flattening of this is further carried out by CMP.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is cross-section structural drawing of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 2] It is cross-section structural drawing showing the 1st process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 3] It is cross-section structural drawing showing the 2nd process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 4] It is cross-section structural drawing showing the 3rd process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 5] It is cross-section structural drawing showing the 4th process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 6] It is cross-section structural drawing showing the 5th process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 7] It is cross-section structural drawing showing the 6th process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 8] It is cross-section structural drawing showing the 7th process of the manufacture method of the semiconductor device concerning the gestalt of operation of the 1st of this invention.
[Drawing 9] It is drawing showing typically an example of the sputtering system used for the gestalt of operation concerning this invention.
[Drawing 10] It is drawing showing the relation of the time and substrate temperature when controlling substrate temperature using the sputtering system shown in drawing 9 .
[Drawing 11] It is drawing showing typically the belt furnace used for the gestalt of operation concerning this invention.
[Description of Notations]
11 Silicon Substrate
12 Field Insulator Layer
13 Gate Oxide Film
14 Gate Electrode
15 Low Concentration Impurity Layer
16 High Concentration Impurity Layer
17 Side-Attachment-Wall Spacer
18 Silicon Oxide
19 Titanium Silicide Layer
20 Layer Insulation Film

38 1st Metal Wiring Layer
40 3rd Silicon Oxide
42 1st Silicon Oxide
44 2nd Silicon Oxide
46 Layer Insulation Film
48 Through Hole
49 Upper Part
50 WETTENGU Layer
51 Lower Part
52 1st Aluminum Film
54 2nd Aluminum Film
62 Antireflection Film
64 2nd Metal Wiring Layer

[Translation done.]